Patent claims

1. An arrangement for interconnection of two or more PCB's communicating with each other over a synchronous data bus, each including a number of loads transferring data in both Rx and Tx direction,
characterized in

a local synchronous data bus in each PCB to which the associated number of loads are connected,

an intermediate CPU controlled logic in each direction connecting a local synchronous data bus to the global synchronous data bus, which logic includes a FIFO buffer through which synchronous data from the local or global data bus is being written in and read out to the local or global data bus introducing a phase difference providing a total delay for any data travelling from a local synchronous bus to the global synchronous data bus and back to a local synchronous data bus being of a controllable dimension.

2. Arrangement as defined in claim 1,
characterized in that the local synchronous data bus is a local TDM data bus and the global synchronous data bus is a global TDM data bus and/or a back plane TDM data bus, and said arrangement is implemented in a circuit switched node

3. Arrangement as defined in claim 1 and 2
characterized in that the total delay is equal to an integer number of data frames.4.Arrangement as defined in claims 2 or 3,
characterized in that the logic further includes a first and a second time slot counter, the first counter addressing a first data location in the FIFO buffer into which, in case of RX direction, time slot data from a local TDM data bus is to be written, or out of

which, in case of TX direction, time slot data to a local TDM bus is to be read, the second counter addressing a second data location in the FIFO buffer into which, in case of TX direction, time slot data from the global TDM bus is to be written, or out of which, in case of RX direction, time slot data to the global TDM bus is to be read, wherein the phase difference between the first and the second time slot counter represents a preferred part of said total delay caused by the logic of the respective direction.

5. Arrangement as defined in claim 4, c h a r a c t e r i z e d i n that the first counter is incremented by a first clock (TDM_CLK LOCAL) corresponding to the current local TDM data bus and initialised by a first frame synchronisation signal (FSYNC LOCAL) indicating the start of each frame in the current local TDM data bus, the second counter is incremented by a second clock (TDM_CLK EXTERN) corresponding to the global TDM data bus and initialised by a second frame synchronisation signal (FSYNC EXTERN) indicating the start of each frame in the global TDM data bus.

6. Arrangement as defined in claim 5, c h a r a c t e r i z e d i n that the first clock and frame synchronisation signal is derived from the second clock and frame synchronisation signal, adapted to provide said preferred part of said total delay caused by the logic of the respective direction.

7. Arrangement as defined in one of the claims 4 - 6, c h a r a c t e r i z e d i n that the logic further includes a table including one bit per data location in the FIFO RAM, wherein, in case of TX direction, if a first logic value (e.g. "1") is assigned to the data location addressed by the first counter, reading of the content in that data location to the certain local TDM data bus is enabled, in contrast to a second logic value (e.g. "0") in

which case reading is disabled, and in case of RX direction, if a first logic value (e.g. "1") is assigned to the data location addressed by the second counter, reading of the content in that data location to the global TDM data bus is enabled, in contrast to a second logic value (e.g. "0") in which case reading is disabled.

8. Arrangement as defined in one of the claims 4 - 7, c h a r a c t e r i z e d i n that the preferred part of said total delay caused by the logic of the RX direction is the duration of one frame minus the preferred part of said total delay caused by the logic of the TX direction.

9. Arrangement as defined in claim 8, c h a r a c t e r i z e d i n that the preferred part of said total delay caused by the logic of the TX direction is the duration of 8 or 16 time slots.

10. Arrangement as defined in one of the preceding claims, c h a r a c t e r i z e d i n that the circuit switched node is a Base Station Controller (BSC) or a switch in any circuit switched enabled data or telecommunication network.